a first programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said read port to conductors in a selected one of said plurality of groups of interconnection conductors; and

a second programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said write port to conductors in said selected one of said plurality of groups of interconnection conductors; wherein:

said first and second programmable interconnection resources are populated to allow connection of an individual conductor in said selected one of said plurality of groups of interconnection conductors to corresponding port conductors in both said read port and said write port.

REMARKS

Summary of Office Action

Claims 1-12 are pending in the above-identified patent application.

The Examiner has finally rejected claims 1-12 under 35 U.S.C. § 102(e) as being anticipated by Heile U.S. Patent 6,020,759. Claims 3-6 and 9-12 have been objected to under 37 C.F.R. § 1.75(c) as being of improper dependent form. The declaration has been objected to as allegedly being defective.

Summary of Applicants' Reply

Applicants have proposed amending claims 3, 4, 9 and 10. The Examiner's objections and rejection are respectfully traversed.

Applicants' Reply to the Objection to Claims 3-6 and 9-12

Claims 3-6 and 9-12 have been objected to under 37 C.F.R. § 1.75(c) as being of improper dependent form.

Applicants have proposed amending claims 3-6 and 9-12 to rewrite them in independent form, and this objection is respectfully traversed.

Independent claims 1 and 7 define, respectively, a programmable logic device ("PLD") and an integrated circuit ("IC"). Claims 3 and 9 define a digital processing system respectively incorporating, inter alia, the PLD of claim 1 or the IC of claim 7. Claims 4-6 and 10-12 define a printed circuit board respectively incorporating, inter alia, the PLD of claim 1 or the IC of claim 7. The basis of the Examiner's objection is not clear, but he seems to be objecting to the fact that the independent and dependent claims are drawn to different types of products.

Applicants and the undersigned are, and have always been, aware of the requirement of 37 C.F.R. § 1.75(c) ("Rule 75(c)") that a dependent claim further limit the subject matter of the claim from which it depends. In the previous Reply to Office Action, applicants attempted to explain to the Examiner why they believe that claims 3-6 and 9-12 as filed qualified as proper dependent claims under Rule 75(c). In particular, applicants pointed out that MPEP § 608.01(n)(III) explicitly permits such dependent claims. For example, in the context of discussing a method claim that depends from a product claim, that section states that "if claim 1 recites a specific product, a claim for the method of making the product of claim 1 in a particular manner would be a proper dependent claim."

According to MPEP § 608.01(n)(III), the only valid test for the propriety of a dependent claim is whether or not the dependent claim could conceivably be infringed by something that would not infringe the independent claim; in a proper claim it could not. Applicants explained in the previous Reply to Office Action why in this case the dependent claim could not conceivably be infringed by something that would not infringe the dependent claim. The Examiner did not address MPEP § 608.01(n) in the final Office Action, and maintained the objection.

Therefore, although applicants continue to believe that claims 3-6 and 9-12 as filed were proper dependent claims, in order to advance prosecution of this application applicants have herein proposed amending claims 3, 4, 9 and 10 by rewriting them in independent form. In the course of rewriting claim 10, applicants observed that claim 10 as filed inadvertently referred to a programmable logic device as defined in claim 7, instead of to an integrated circuit as defined in claim 7, and has corrected that as well. Applicants respectfully submit that these amendments, which do not change the substance of the claims, are not "substantial amendments related to patentability" within the meaning of Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd., 234 F.3d 558, 56 USPQ2d 1865 (Fed. Cir. 2000), but instead relate merely to matters of form.

Applicants respectfully submit that claims 3-6 and 9-12, as amended, are in proper form, and respectfully request that the objection to claims 3-6 and 9-12 be withdrawn.

Applicants' Reply to the
Objection to the Declaration

The declaration filed with the above-identified patent application has been objected to as allegedly being defective for not identifying the citizenship or residence of each inventor. This objection is respectfully traversed.

In the previous Reply to Office Action, the undersigned quoted from the declaration ***as originally filed***, to show where the declaration included the recitations that were alleged to have been missing therefrom. The Examiner in his final Office Action apparently misunderstood the undersigned's quotation from the declaration as an attempt to amend the declaration. However, the undersigned has always been aware that the declaration cannot be amended and was not attempting to do so.

To reiterate, the declaration ***as filed with the above-identified patent application*** states, in the first paragraph:

We, Tony K. Ngai, Rakesh H. Patel, Srinivas T. Reddy, and Richard G. Cliff, declare that we are citizens, respectively, of Canada, the United States of America, India, and the United States of America, respectively residing and having post office addresses at 2830 Gazelle Drive, Campbell, California 95008, 20087 Las Ondas Court, Cupertino, California 95104, 2289 Camellia Court, Fremont, California 94539, and 194 Smithwood Street, Milpitas, California 95035.

The Examiner is encouraged to inspect the declaration in the Patent and Trademark Office file of this application. It will be apparent that the above-quoted paragraph, which identifies the citizenship, residence and post office address of each applicant as required, ***was in the declaration as of the filing date of the above-identified patent application***. Accordingly, applicants respectfully request that the objection to the declaration be withdrawn.

Applicants' Reply to the
Prior Art Rejection

Claims 1-12 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Heile U.S. Patent 6,020,759. This rejection is respectfully traversed.

Applicants in the previous Reply to Office Action explained the functions of both (1) applicants' invention, and (2) that which is disclosed by Heile, as background to enable the Examiner to understand the specific differences between the subject matter of Heile and the subject matter of applicants' claims. The Examiner in the final Office Action has apparently focused on the applicants' general background discussion and not on the specific differences between the subject matter of Heile and applicants' claims. Accordingly, applicants herein reiterate those differences.

The Examiner correctly equates the claimed plurality of interconnection conductors with conductor

network 23 of Heile. The Examiner then purports to identify the claimed plurality of programmable interconnection resources -- for connecting conductors of the interconnection conductors 23 to the plurality of logic resources 21, and including the claimed first and second programmable interconnection resources -- with the decoders and multiplexers 13, 18, 19, 103 and 107. However, even if those decoders and multiplexers had all of the other characteristics that the claims require of the claimed programmable interconnection resources, the decoders and multiplexers do not connect to Heile's conductor network 23, but rather to conductors within Heile's RAM module 10. Accordingly, Heile does not anticipate applicants' claims, which require that the programmable interconnection resources (according to the Examiner, Heile's decoders and multiplexers) connect "conductors in said groups of interconnection conductors [(according to the Examiner, Heile's conductor network 23)] to one another and to said plurality of logic resources."

In addition, applicants' claims require:

> a first programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said read port ***to a selected one*** of said plurality of groups of interconnection conductors; and
>
> a second programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said write port ***to said selected one*** of said plurality of groups of interconnection conductors [emphasis added].

Heile does not meet these limitations either. Heile does not show that a particular one of the programmable interconnection resources (i.e., according to the Examiner, a particular multiplexer or decoder) connects read port conductors to a particular one (i.e., "a selected one" in applicants' claims) of the conductors in Heile's conductor network 23, while another one of the interconnection resources connects write port conductors to ***the same one***

(i.e., "***said*** selected one" in applicants' claims) of the conductors. According to FIGS. 1 and 5 of Heile, it appears that the DATAOUT conductors ("read port" conductors according to the Examiner) and the DATAIN conductors ("write port" conductors according to the Examiner) are connected to different places; there is certainly no teaching that they are connected to the same place.

Also, applicants claims specify that the interconnection resources are less than fully populated. As is well-known in programmable logic devices, a "less than fully populated" interconnection resource allows each conductor in one group of conductors to access at least one conductor in a second group of conductors, as compared to a fully populated resource which allows every conductor in the first group to reach every conductor in the second group.

Heile does not show less-than-fully-populated interconnection resources as claimed by applicants. The Examiner points to column 3, line 50 through column 4, line 12 of Heile as supporting the claimed limitations on the degree to which the first and second programmable interconnection resources are populated. This portion of Heile discusses only the re-routing of the normal read address lines to the p-term inputs, neither of which connects to either the read port or the write port as do the claimed first and second programmable interconnection resource. And even though the address decoders of Heile have more outputs than they have inputs, there is no teaching or suggestion in Heile that those decoders do not allow every input to reach every output.

Finally, according to applicants' claims, even though the interconnection resources are less than fully populated, they are sufficiently populated to allow a particular interconnection conductor to be connected to corresponding conductors in both the read port and the write port (so as to enable emulation of single-port operation). Again, there is no teaching or suggestion in Heile of this limitation. Indeed, there is no teaching or suggestion that

any DATAIN conductors are connected through the interconnection conductors to any DATAOUT conductors, let alone that corresponding DATAIN and DATAOUT conductors are connected to each other through the interconnection conductors.

An anticipation rejection under any subsection of 35 U.S.C. § 102, including Section 102(e), requires that all of the limitations of applicants' claims be found in the allegedly anticipating reference. Applicants have shown that Heile does not show all of the elements of applicants' claims. Specifically, as discussed above, Heile does not show (1) programmable interconnection resources that connect conductors in said groups of interconnection conductors to one another and to said plurality of logic resources, (2) a first programmable interconnection resource for connecting port conductors in said read port ***to a selected one*** of said plurality of groups of interconnection conductors and a second programmable interconnection resource in said plurality of programmable interconnection resources for connecting port conductors in said write port ***to said selected one*** of said plurality of groups of interconnection conductors, or (3) interconnection resources that are less than fully populated, but (4) are sufficiently populated to allow a particular interconnection conductor to be connected to corresponding conductors in both the read port and the write port. Heile also does not suggest applicants' invention.

For these reasons, applicants respectfully submit that the claimed invention is patentable.

Conclusion

For the reasons set forth above, applicants respectfully submit that this application, if amended as proposed, is in condition for allowance. Reconsideration,

entry of the proposed amendments, and prompt allowance of this application are respectfully requested.

Respectfully submitted,

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